Remarks

The above Amendments and these Remarks are in reply to the outstanding Office Action in the above-identified patent application. Claims 1-181 are currently pending with claims 15-179 withdrawn.

Claims 6-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 5 and 180-181 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,631,486 (*Komatsu et al.*).

Claims 2-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Komatsu et al.* in view of U.S. Patent No. 7,092,637 (*Haruyama*).

I. Rejection of Claims 1, 5 and 180-181 under 35 U.S.C. §102(e)

Claims 1, 5 and 180-181 are rejected under 35 U.S.C. §102(e) as being anticipated by *Komatsu et al.*

Independent claims 1 and 180-181 calls for specifically claimed elements in a single "semiconductor device" or "device." Previous office actions have admitted that *Komatsu et al.* does not disclose a single "semiconductor device comprising..."

The current Office Action at page 4 now states:

> The Examiner [is, sic] now using [a, sic] second embodiment of Komatsu et al. to reject claims 1-5 and 180-181, wherein in column 7, lines 53-55 wherein tester and DUT are in the same semiconductor structure.

However, column 7, lines 53-55 of *Komatsu et al.* does not describe that the tester and DUT are in the same semiconductor structure. In contrast, this passage explicitly implies they are separate devices by referring to the first embodiment:

> In the other respects, the DUT 20' and the tester 10 **are the same as the counterparts according to the first embodiment**. That is to say, the high-speed transmitter 22 transmits the…Col. 7, lines 53-55. (Emphasis added.)

Turning to the description of the referenced first embodiment ("EMBODIMENT 1"), *Komatsu et al.* states:

> FIG. 1 illustrates an overall block arrangement for testing a semiconductor integrated circuit according to a first embodiment of the present invention. Specifically, the semiconductor integrated circuit, or a device under test (DUT) 20, is tested using a tester 10. Col. 5, lines 63-67.

Thus, *Komatsu et al.* discloses in the second embodiment, by reference to the first embodiment, a separate "semiconductor integrated circuit" and "tester 10" or that "tester 10" is not included in semiconductor integrated circuit 20.

Therefore it is respectfully requested that the rejection of claims 1, 5 and 180-181 under 35 U.S.C. §102(e) be withdrawn.

II. Rejection of Claims 2-4 under 35 U.S.C. § 103(a)

Claims 2-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Komatsu et al.* in view of *Haruyama*.

Claims 2-4 depend from independent claim 1 and therefore are patentable for at least the reasons stated above in regard to claim 1.

Therefore it is respectfully requested that the rejection of claims 2-4 under 35 U.S.C. § 103(a) be withdrawn.

III. Conclusion

Based on the above Amendments and these Remarks, reconsideration of claims 1-14 and 180-181 is respectfully requested.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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